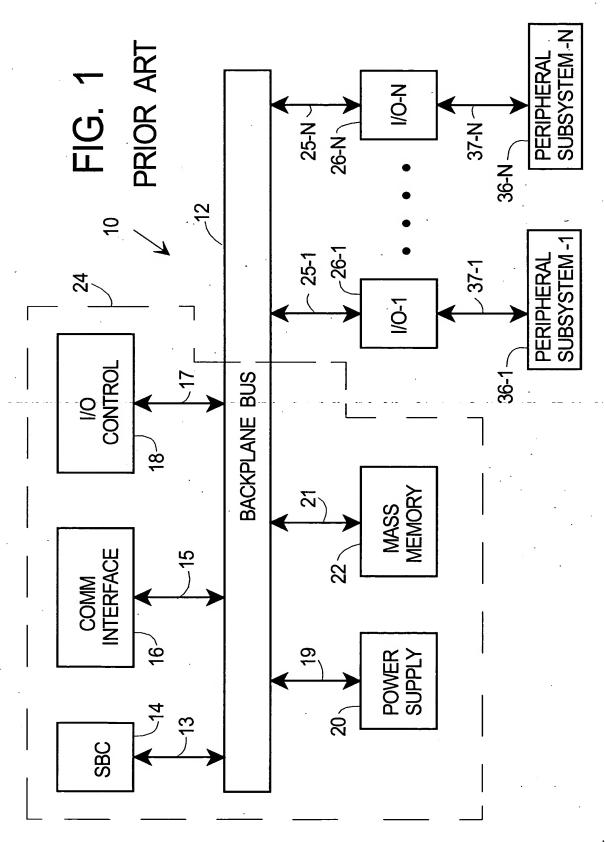
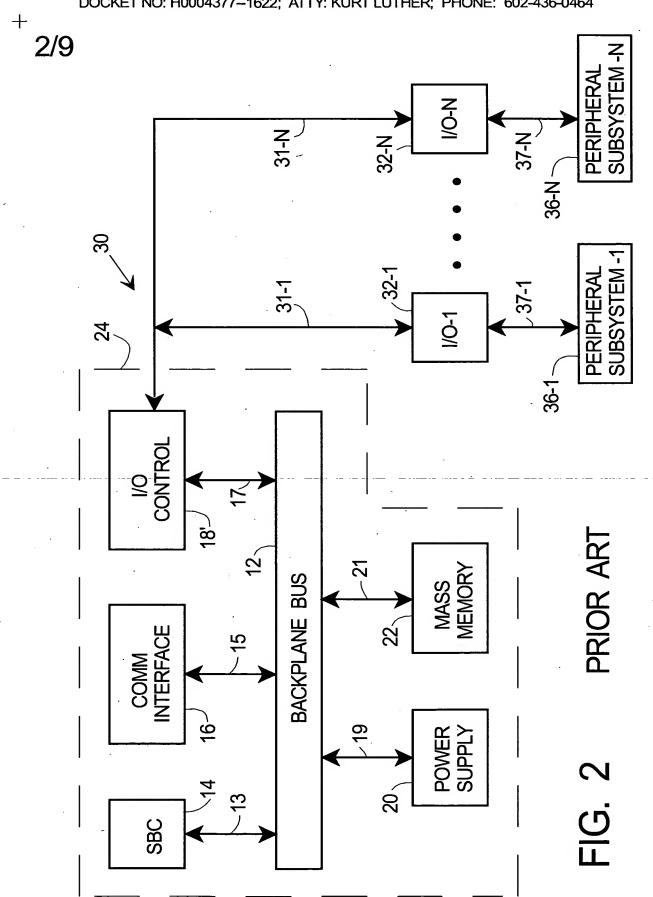
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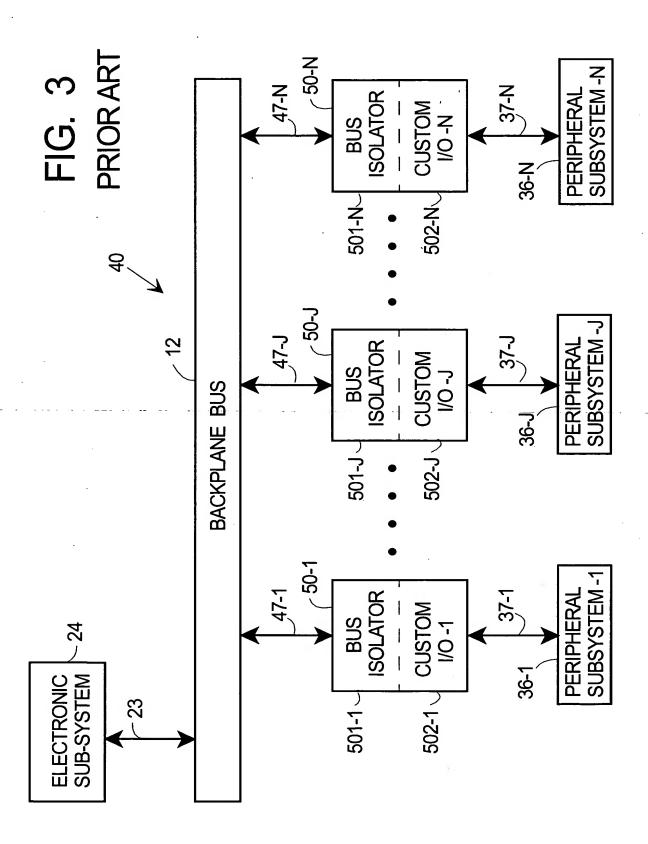


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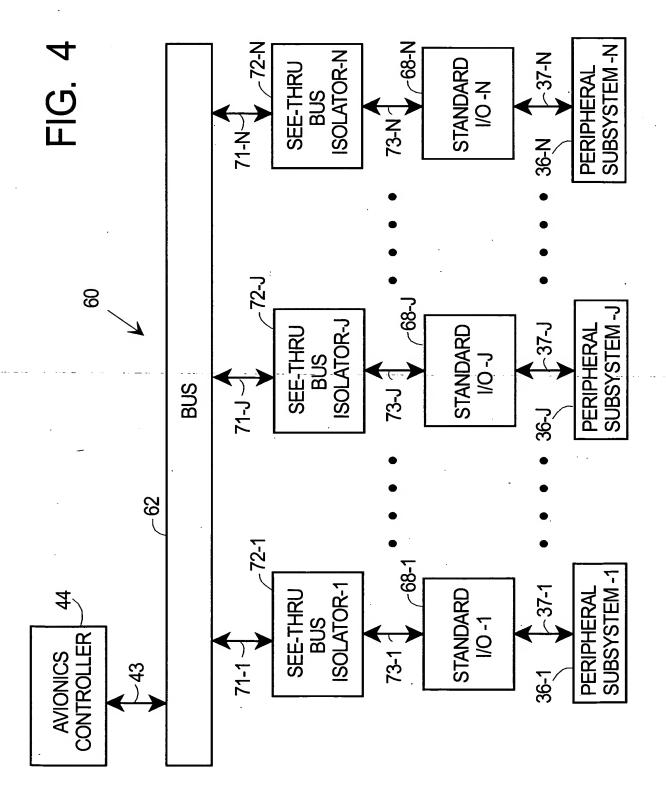
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BUS 71-J 62 **TARGET** 84 INTERFACE 90 86 91 **MEMORY** CONTROLLER 97 c 92 PROCESSOR 87-95 88 DEBUG 94 **MASTER** PORT **INTERFACE** 72-J ~73-J STANDARD 68-J I/O - J 60 37-J 36-J **PERIPHERAL** SUBSYSTEM - J

FIG. 5

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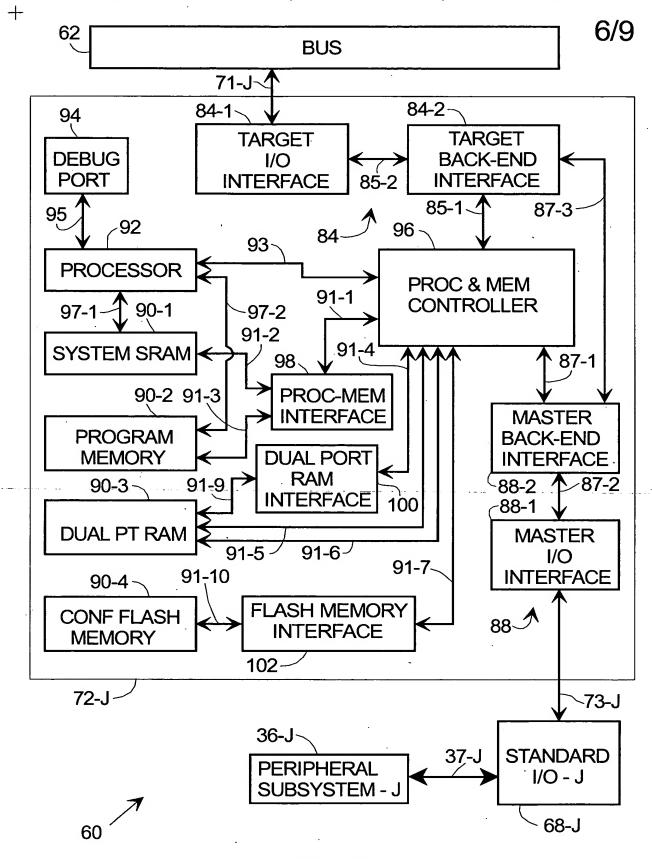


FIG. 6

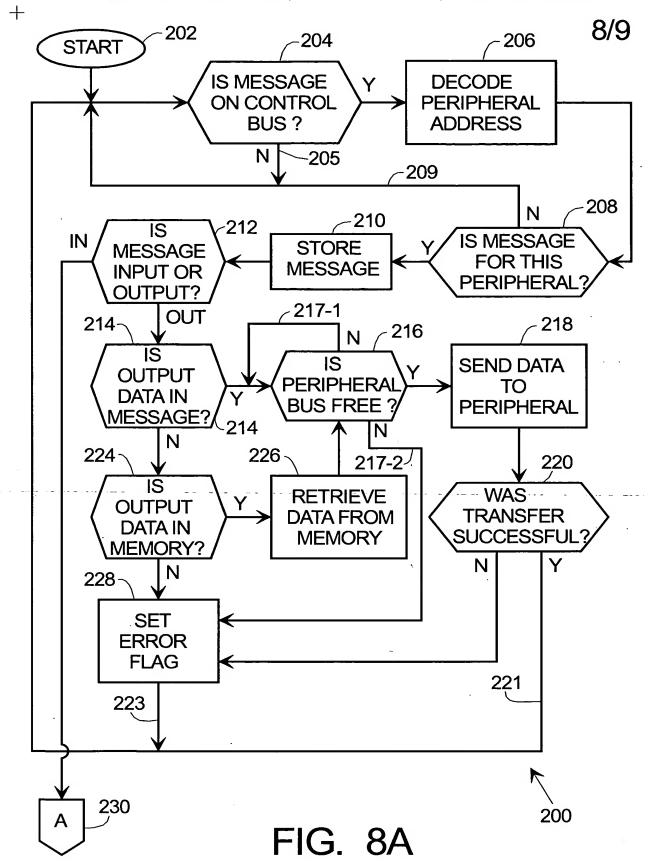
INVENTORS: MITCHELL S. FLETCHER, ET AL

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DOCKET NO: H0004377--1622; ATTY: KURT LUTHER; PHONE: 602-436-0464

BUS 62 -121-X 121-Y-143 X-LANE Y-LANE 142 143-2 **LOCK STEP LOCK STEP** PROCESSOR | **PROCESSOR** 143-1 -142-X 142-Y-141-Y1 Y-LANE 122-J - 141-X **BUFFER** 145 141-Y2 140-X 140-Y 137 X-LANE Y-LANE CONTROL CONTROL 135-X 135-Y 130-2 131-Y 139-X 139-Y 131-X PCI I/O MACRO **BACK-END INTERFACE** *-*133 130-1 132-X-- 132-Y X-LANE DUAL PCI I/O MACRO Y-LANE DUAL 130 PORT RAM MASTER INTERFACE PORT RAM 73-J 37-J **STANDARD** 68-J 120 1/0 36-J **PERIPHERAL** FIG. 7 **SUBSYSTEM**

INVENTORS: MITCHELL'S. FLETCHER, ET AL



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